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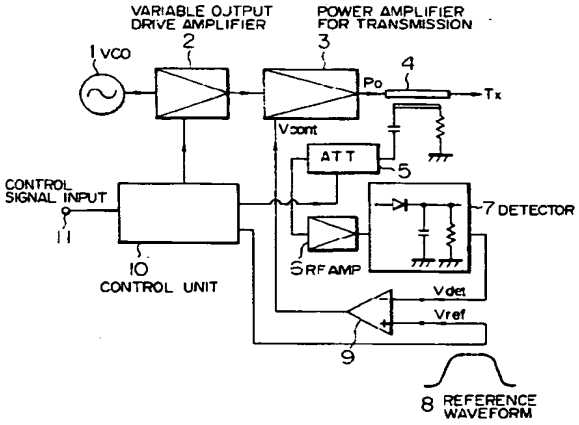
(54) Control circuit and method for transmission output.

(57) A control circuit for a transmission output is used in a TDMA system radio transmitter or the like and can control a transmission output burst wave stably with high accuracy over a wide range. There is provided a closed loop system (3 - 7, 9) in which part of the transmission output is taken out and detected to be compared with a reference voltage to control a power amplifier (3) and an open loop system (2, 10) for controlling a drive amplifier (2) connected to an input of the power amplifier, so that a wide range operation of the transmission output and multi-stage control are attained by combining controls of both the loops.

FIG. 1



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BACKGROUND OF THE INVENTION

The present invention relates to a control circuit for a transmission output of a radio transmitter or the like, and more particularly, to a control circuit suitable for a TDMA transmitter requiring stable control with high precision over a wide dynamic range.

Heretofore, the control circuit for the transmission output of this type frequently uses a closed-loop system which detects part of the transmission output to feed the detected output back to a power amplifier (for example, U.S. Patent No. 4, 602, 218).

The control circuit for the transmission output as shown in Figs. 11 and 12, for example, are known.

In Fig. 11, an output signal produced by an oscillation source 1 is supplied to a power amplifier 3 (power amplifier system) to drive the power amplifier so that a transmission output (TX) is obtained. Part of the transmission output is taken out by a directional coupler 4 and is detected by a detector 7. A detected output (Vdet) of the detector 7 is compared with a reference output (Vref) in a comparison error amplifier 9 and an output of the comparison error amplifier 9 controls the power amplifier 3 as a control voltage (Vcont). In this manner, a feedback system (detection system) is formed. Numeral 8 represents a waveform of a reference output in the form of burst.

Further, in Japanese Patent Application No. 2-219215 (JP-A-4-100426) shown in Fig. 12, a variable attenuator 5 is connected between the directional coupler 4 and the detector 7 to vary an amount of attenuation of the variable attenuator 5 in accordance with a value of the transmission output, so that an input level of the detector 7 is maintained constant so that the detection system can attain stable control over a wide dynamic range.

However, in the first conventional circuit shown in Fig. 11, when it is applied to a TDMA transmitter to produce the transmission output in the form of burst, it is difficult to make short rising and falling characteristics of the transmission output and adjust the transmission output over a wide range since dynamic ranges of both of the detection system and the power amplifier system are narrow. Further, there is a problem that the stability including a temperature characteristic of an output is lacking in a small output.

In the second conventional circuit configuration shown in Fig. 12, a dynamic range of control of the detection system is broadened and accordingly the stability and the reproducibility are improved, while since a dynamic range of the power amplifier system is the same as that of Fig. 11, there is a problem that overshoot and unnecessary oscillation occur in rising of the burst output. Further, the stability of a temperature characteristic of the transmission output is not sufficient.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above problems in the prior art and to provide a control circuit for a transmission output which can attain control from a low output to a high output with high accuracy and obtain a transmission burst output having high-degree stability and reproducibility.

In order to achieve the above object, according to the present invention, a drive stage having a variable output is provided before the power amplifier and an output of the power amplifier is detected through variable amplifier means. The detected output is compared with a reference voltage to control the power amplifier in accordance with an error voltage produced by the comparison. Further, the drive stage, the variable amplifier means and the reference voltage are controlled by a control signal corresponding to a desired transmission output.

According to the present invention, since both of a power amplifier system including a drive amplifier and a detection system are controlled independently in accordance with the transmission output as an open loop for the former and as a closed loop for the latter, respectively, the dynamic ranges of both the systems are broadened and control with high accuracy and high stability can be attained over a wide range of the output.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a control apparatus for a transmission output according to an embodiment of the present invention;

Fig. 2 is a waveform diagram illustrating characteristics of the apparatus of Fig. 1;

Fig. 3 is a diagram illustrating an output characteristic versus an ideal control voltage of the apparatus of Fig. 1;

Fig. 4 is a diagram illustrating output characteristics versus an actually measured control voltage of the apparatus of Fig. 1;

Fig. 5 is a diagram illustrating temperature characteristics of the output of the apparatus of Fig. 1;

Fig. 6 is a block diagram schematically illustrating a configuration of a variable output drive amplifier of the apparatus of Fig. 1;

Fig. 7 is a characteristic diagram illustrating a relation of an output and a gate control voltage of the apparatus of Fig. 1;

Fig. 8 is a characteristic diagram illustrating a relation of an optimum drive level and a transmission output of the apparatus of Fig. 1;

Fig. 9 is a diagram schematically illustrating another configuration example of a control unit;

Fig. 10 is a diagram schematically illustrating another configuration example of a drive stage;

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Fig. 11 is a block diagram schematically illustrating a configuration example of a conventional control circuit for a transmission output; and
Fig. 12 is a block diagram schematically illustrating a configuration example of another conventional control circuit of a transmission output.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 schematically illustrates an embodiment of the present invention. In Fig. 1, numeral 1 denotes an oscillation source of a transmission output including a VCO (voltage control oscillator), 2 a variable output drive amplifier described later, 3 a power amplifier (for transmission), 4 a directional coupler, 5 a variable attenuator (ATT) of which an attenuation factor is controlled by a control unit 10, 6 a high-frequency amplifier (RFAMP), 7 a detector including a diode, 9 a comparison error amplifier for comparing an output (Vdet) of the detector 7 with a reference voltage (Vref), 10 a control unit which controls the variable output drive amplifier 2, the ATT 5 and the reference voltage (Vref) in accordance with a control signal input 11, and 8 a burst reference waveform.

Operation is now described with reference to Figs. 1 to 4. In Fig. 1, part of an output of the power amplifier 3 is derived from the directional coupler 4 and is supplied to the ATT 5. The attenuation factor of the ATT 5 is controlled to be varied in accordance with a digital control signal of four bits, for example, supplied as the control signal input 11 through the control unit 10. Such a digital control signal is frequently sent from a base station (e.g., a station for mobile communication) and is decoded in the control unit. An output of the ATT 5 is supplied through the high-frequency amplifier 6 to the detector 7. At this time, the attenuation factor of the ATT 5 and the amplification degree of the high-frequency amplifier 6 are controlled to make an input supplied to the detector 7 constant regardless of the transmission output (Po). An output (Vdet) of the detector 7 and the reference voltage (Vref) are successively compared in the comparison error amplifier 9 composed of a comparator and an output of the power amplifier 3 is controlled by an error voltage (Vcont) of the comparison error amplifier 9. In this manner, the directional coupler 4, the variable attenuator 5, the high-frequency amplifier 6, the detector 7, the comparison error amplifier 9 and the power amplifier 3 constitute a closed feedback loop for the detection system. The reference voltage (Vref) is of a burst form as shown by the reference waveform 8 and is supplied to the control unit 10 as a voltage having a peak value varying in response to the transmission output Po.

On the other hand, as the reference voltage of the comparison error amplifier, a control signal having a rising and falling waveform of the transmission burst wave is applied. More particularly, as shown in Fig. 9, data stored previously in a ROM 22 of a control unit 20 is read out in synchronism with a transmission timing and is supplied through a D-A converter 23 as an analog waveform signal. Accordingly, for example, if all of transmission output level information are applied as digital control signals, the burst waveform control signal is fixed and the ROM can be economized. In Fig. 9, a CPU 21 is used in the control unit 21.

Further, the ATT 5 and the high-frequency amplifier 6 constitute a variable amplifier. The high-frequency amplifier 6 constituting the variable amplifier in the feedback loop can be omitted if a sufficiently large detection voltage can be derived.

Fig. 4 shows an output control characteristic of the power amplifier 3 measured while an input drive level is varied. If a degree of variation of an output to a control voltage is defined as a control sensitivity, it is desirable that the control sensitivity is fixed regardless of the output in order to broaden the dynamic range. For example, if the drive level is changed to that corresponding to the curve (b) from the curve (a) of Fig. 4 correspondingly when the output is required to be reduced by 10 dB, the control sensitivity is not changed. Further, when the output is required to be reduced by 24 dB, the drive level is changed to that corresponding to the curve (c) to maintain the control sensitivity to be fixed.

When the drive levels satisfying such a condition are obtained for each output level and values thereof are supplied to the power amplifier 3 as drive inputs, a lumping waveform of the output burst is improved as shown in Fig. 2. Overshoot and unnecessary oscillation are improved, the same control sensitivity is maintained for all power level basically, and the operation level of the detection system is also fixed.

Particularly, when the operation level of the detection diode is fixed and the detected voltage is also used in several volts at the maximum, the output control is extremely stable and the dependency on temperature in surroundings is very small, so that there is a large merit that temperature compensation is not required over all output levels. Generally, a relation of a forward current and voltage of a diode is influenced by a voltage drop by an internal resistance of the diode in a large current area, while since the voltage drop possesses a positive temperature coefficient which is canceled by a negative temperature coefficient of the forward current, there is a tendency that the influence is effectively small and use in the large current are is desirable.

On the other hand, the control sensitivity of the power amplifier system is considered as another element of the control system. When a relation of the output versus the control voltage is fixed with straight slope as shown in Fig. 3, the control sensitivity of the power amplifier is fixed regardless of the output and is coincident with the fixed control sensitivity of the

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detection system, so that the transmission output can be controlled only by the closed loop composed of the power amplifier system, the detection system and the comparison error amplifier over a wide dynamic range from small power to large power. However, generally, a relation of the output versus the control voltage of the power amplifier is saturated in the vicinity of the maximum output as shown by the curve (a) of Fig. 4 and the control sensitivities of the output levels, that is, tangential lines are varied greatly. Particularly, when the output is reduced, the control sensitivity is suddenly increased and oscillation occurs in the control loop. The oscillation in the closed loop can be stopped by slowing the response of the loop, whereas the burst waveform can not be controlled in the vicinity of the maximum power and effect of automatic output control (APC) for variation in the supply voltage and the input level can be expected.

Fig. 6 schematically illustrates an actual configuration of the variable output drive amplifier 2. The drive amplifier includes matching circuits provided at input and output sides and an intermediate portion and two cascade-connected FET's connected between the respective matching circuits. An RF signal is supplied to a first gate G1 of the respective FET's which is held at a fixed bias and a second gate G2 is used as a control terminal. A level variation amount per transistor is 15 to 20 dB and two-stage configuration is adopted in order to vary the level by 30 dB or more by way of example. A MOS dual gate FET is best as an FET element if importance is attached to the IM distortion of the amplifier, while a GaAs dual gate amplifier may be used as a mere level variable amplifier. Generally, when the control current is extremely reduced, it may be a gate controlled FET amplifier. If a mere current booster is provided to attain the collector voltage control, the control range, the reality and the stability are deteriorated and there is almost no merit.

Fig. 7 is a graph showing a characteristic of an output level versus a gate voltage in the two-stage dual-gate FET configuration.

On the other hand, the optimum drive input level to the output levels of the power amplifier 3 is varied with a relation as shown in Fig. 8, for example, and there is an allowable width in this value to a certain extent. More particularly, the optimum drive level to the transmission output level is not required to be set to a specific level strictly, while it is desirable that the optimum drive level is set within a predetermined range.

The variable output drive amplifier 2 is supplied with a gate bias in accordance with the output level by means of designation from the control unit 10, while as an embodiment, when the output level information is given by 4-bit digital value, a circuit including a D-A converter constituted by a simple operational amplifier as shown in Fig. 6 may be used. An OR circuit of Fig. 6 serves to increase the drive level at the highest output level. D0, D1 indicate upper bits, which take low level for high power output levels. The D-A conversion characteristic is adapted to increase the analog output particularly for such high power output levels. With such a configuration, the rapidly increased optimum drive level upon the high transmission output as shown in Fig. 8 can be treated.

On the contrary, the amplification degree of the drive amplifier is suppressed upon the low output and the drive amplifier operates as an attenuator rather than an amplifier. An example of such a drive stage is shown in Fig. 10. In Fig. 10, numeral 22 denotes a variable attenuator. Further, when strictness is required for the dynamic range, the variable attenuator 22 and the variable output drive amplifier 2 may be switched in accordance with the output level.

Such a variable output drive amplifier 2 is connected to the input of the power amplifier 3 to attain the open loop control, so that the control sensitivity of the power amplifier can be maintained substantially constant and stable transmission burst waveform control can be attained over all output levels.

When an input level of the drive amplifier 2 is 0 dB, the level distribution of the input (Pin) and the output (Pout) of the power amplifier 3 upon the optimum minimum output and maximum output is as follows:

Po	Pin
15dBm	-25dBm
41dBm	6dBm

As apparent from the above embodiment, according to the present invention, two sets of loops having the closed loop control in which the variable attenuator is connected after the transmission output coupler to maintain the control sensitivity of the detection system to be constant with respect to variation of the transmission output and the open loop control in which the variable output level drive amplifier is connected before the power amplifier to open-loop control the drive level are combined, so that the transmission output can be controlled with a constant control sensitivity over all output level. Consequently, not only control over a wide range of the transmission output level but also high-speed control over a wide dynamic range such as waveform control of rising and falling of the transmission burst waveform are possible. Further, since the operation level of the detection system is constant, there are large effects that operation is very stable, the reproducibility is high, the dependency on temperature in surroundings is small and the temperature compensation is not required over all output level. In addition, unnecessary oscillation occurring generally in small transmission power is not produced according to the present invention

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and high-speed and stable control is possible.

Claims

1. A control circuit for a transmission output comprising a feedback loop including a variable output drive stage (2) driven by a high-frequency signal from an oscillation source (1), a power amplifier (3) cascadeconnected to said variable drive stage to obtain the transmission output, a directional coupler (4) for detecting part of the transmission output and a detector (7) supplied with the detected output through a variable amplifier (5, 6) and having an output being compared with a reference voltage source for controlling said power amplifier in accordance with an error voltage produced by said comparison, and a control unit (10) supplied with a control signal corresponding to a desired transmission output to control said variable amplifier, said reference voltage source and said drive amplifier by an output of said control unit.

2. A control circuit for a transmission output according to Claim 1, wherein said variable amplifier (5, 6) includes a variable attenuator (5) controlled by said control unit (10).

3. A control circuit for a transmission output according to Claim 1, wherein said variable amplifier (5, 6) includes a high-frequency amplifier (6) having a fixed amplification degree.

4. A control circuit for a transmission output according to Claim 1, wherein said control unit (10) includes compensation means for increasing an output of said drive amplifier upon a high transmission output as compared with upon a low transmission output.

5. A control circuit for a transmission output according to Claim 1, wherein said control unit (10) includes a digital circuit and a digital-to-analog converter for converting an output of said digital circuit into an analog control signal.

6. A control circuit for a transmission output according to Claim 1, wherein said drive amplifier (2) includes a plurality of cascade-connected FET amplifier circuits (FET's 1 and 2) and an amplification degree of at least one of said FET amplifier circuits is controlled by said control unit.

7. A control circuit for a transmission output according to Claim 6, wherein a dual gate FET is used as an FET of said FET amplifier circuit.

8. A control circuit for a transmission output according to Claim 1, wherein said reference voltage is produced by writing a waveform control signal upon rising and falling of a transmission burst wave into a ROM attached to said control unit as data and reading the data in synchronism with a transmission timing to convert it into an analog signal.

9. A control circuit for a transmission output according to Claim 1, wherein a desired transmission output information is derived by receiving and decoding an electric wave for command from a base station.

10. A control circuit according to Claim 1, wherein said drive means includes an amplifier.

11. A control method for a transmission output comprising closed loop means including a variable drive stage (2) driven by a high-frequency signal from an oscillation source and a power amplifier (3) cascadeconnected to said variable drive stage to obtain the transmission output, part of the transmission output being detected, said detected output being compared with a reference voltage corresponding to a desired transmission output to control said power amplifier by an error voltage produced by the comparison, and open loop means for controlling an output level of said drive amplifier to be substantially constant in accordance with said reference voltage regardless of variation of the transmission output.

12. A method according to Claim 11, wherein a desired transmission output information is derived by receiving and decoding an electric wave for command from a base station.

13. A method according to Claim 11, wherein said drive means includes an amplifier.

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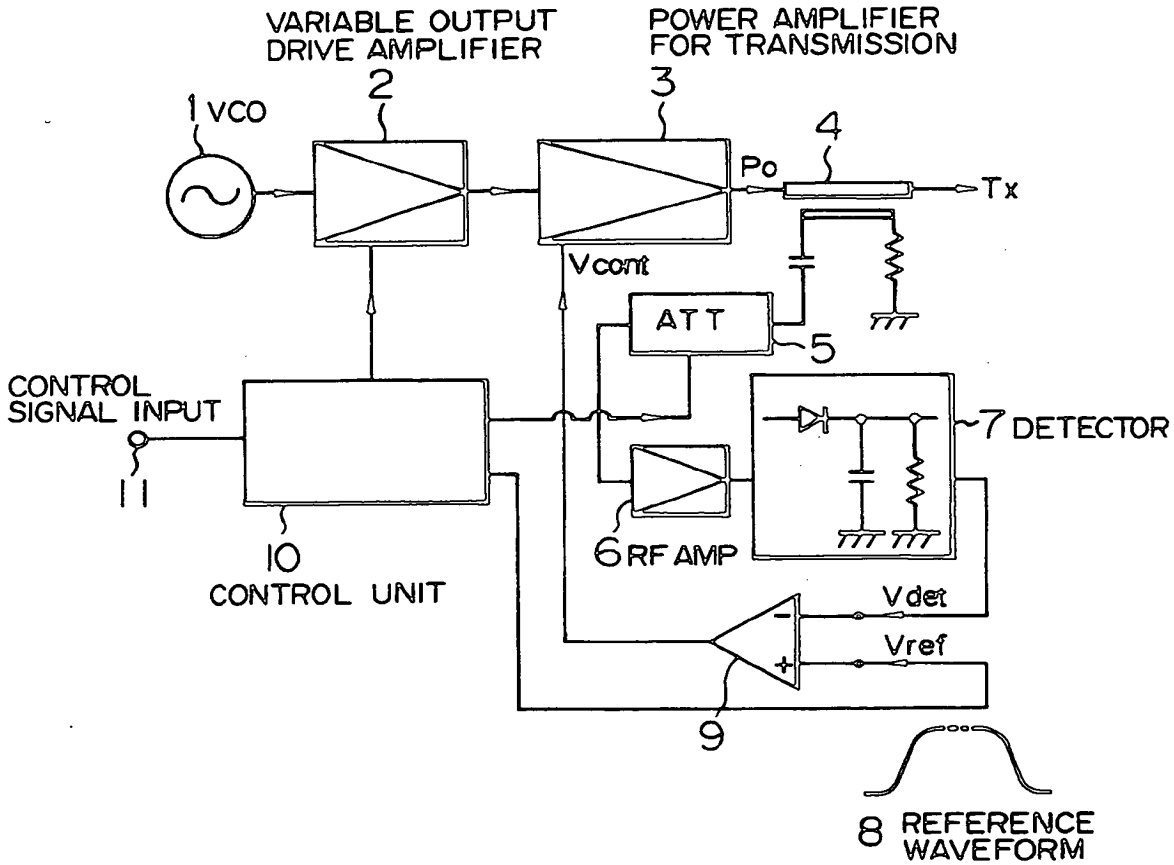
FIG. 1



BNSDOCID: <EP__0546693A1_I_>

FIG. 2

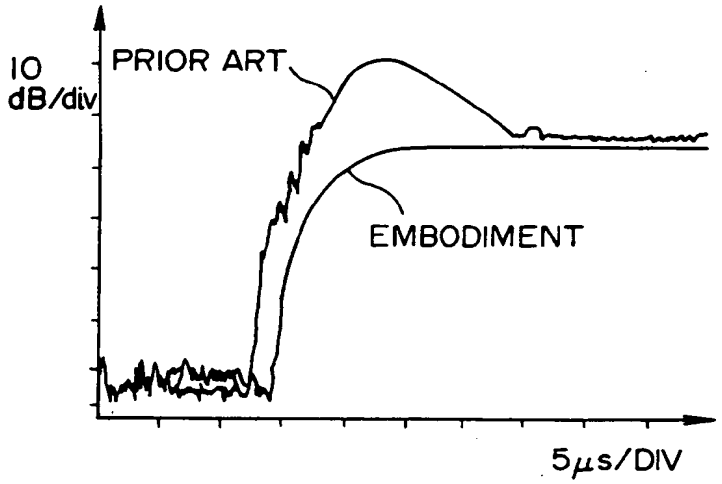


FIG. 3

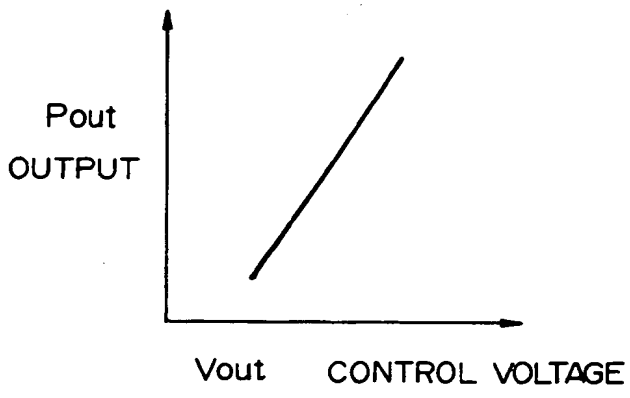


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FIG. 4

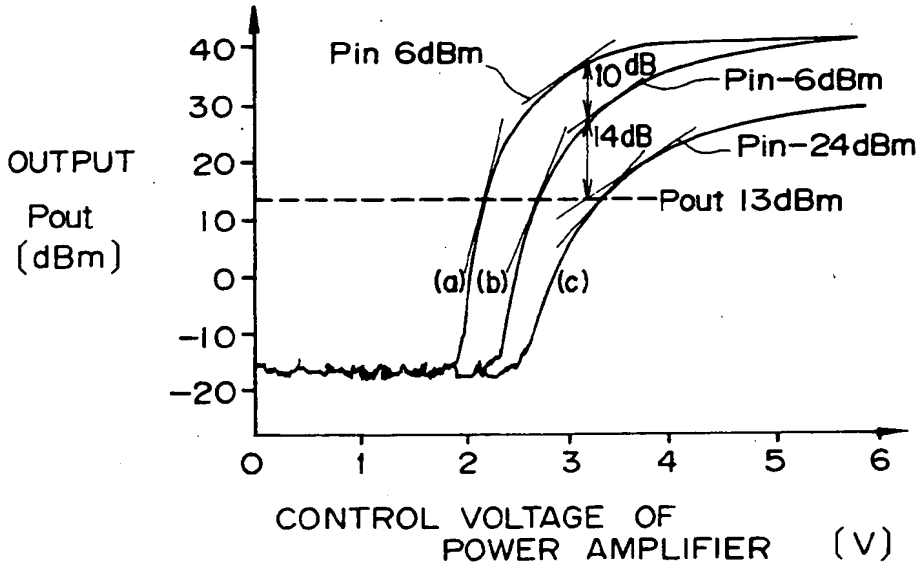
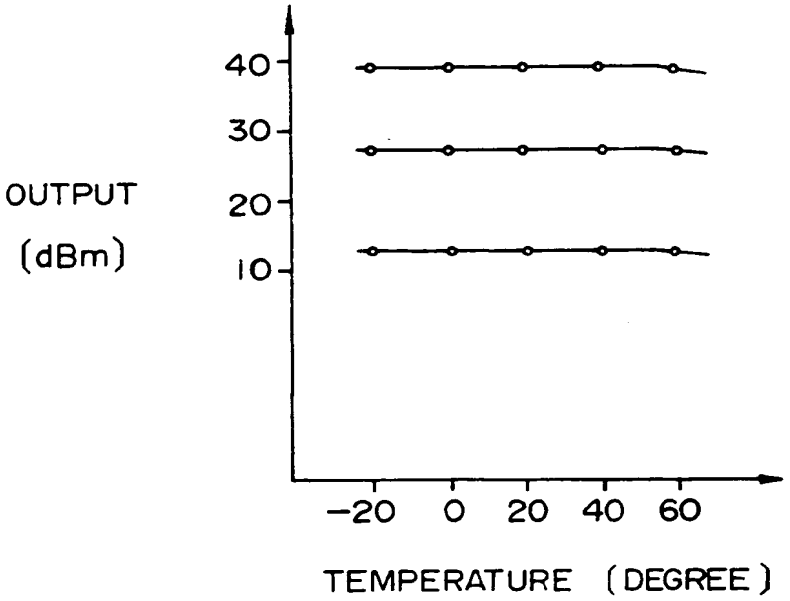


FIG. 5



BNSDOCID: <EP__0546693A1_I_>

FIG. 6

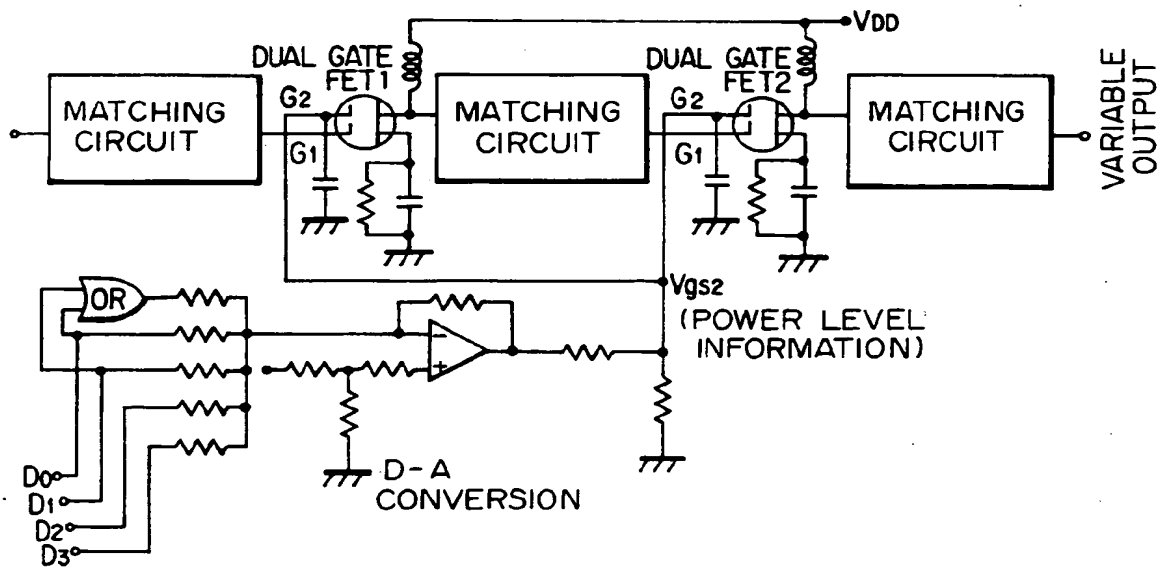


FIG. 7

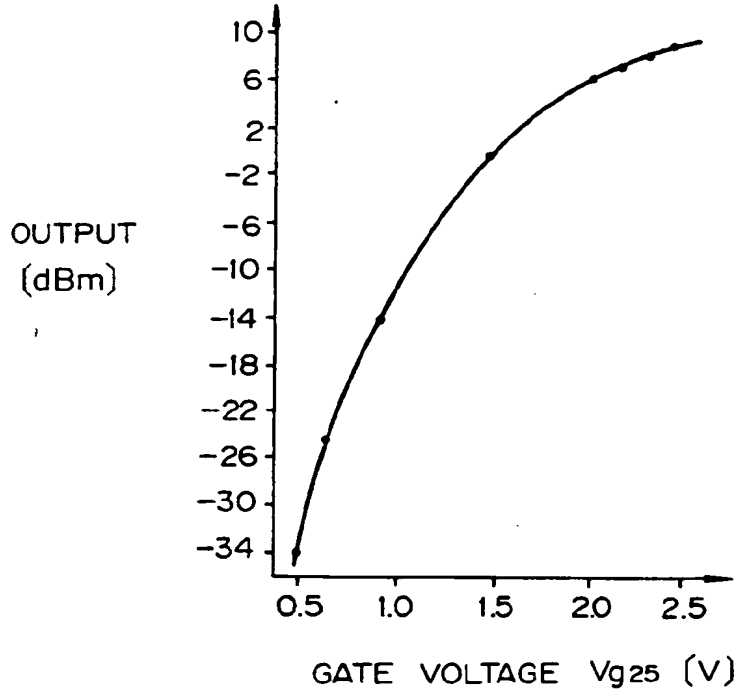


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FIG. 8

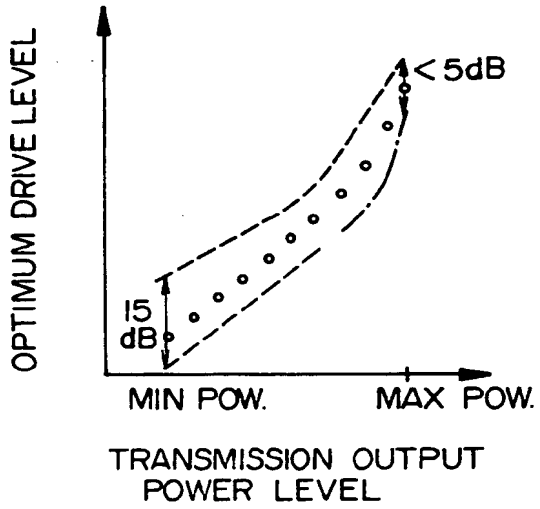

FIG. 9

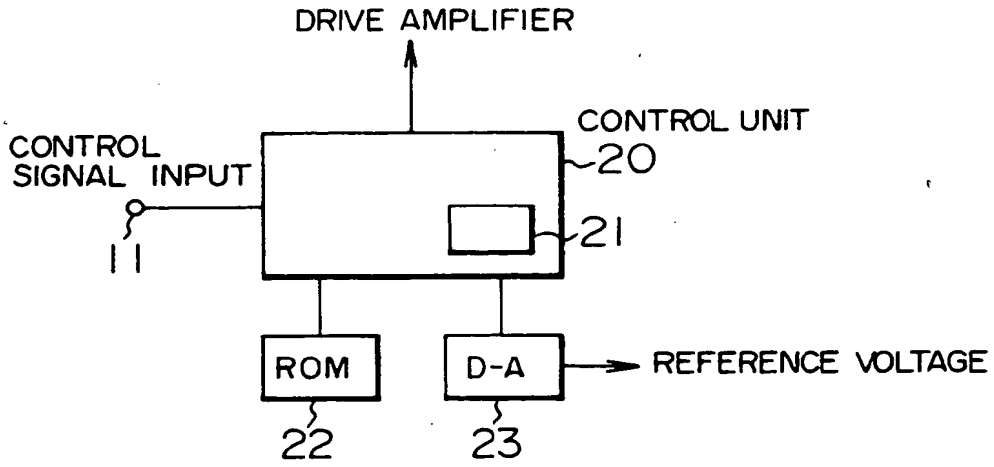

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FIG. 10

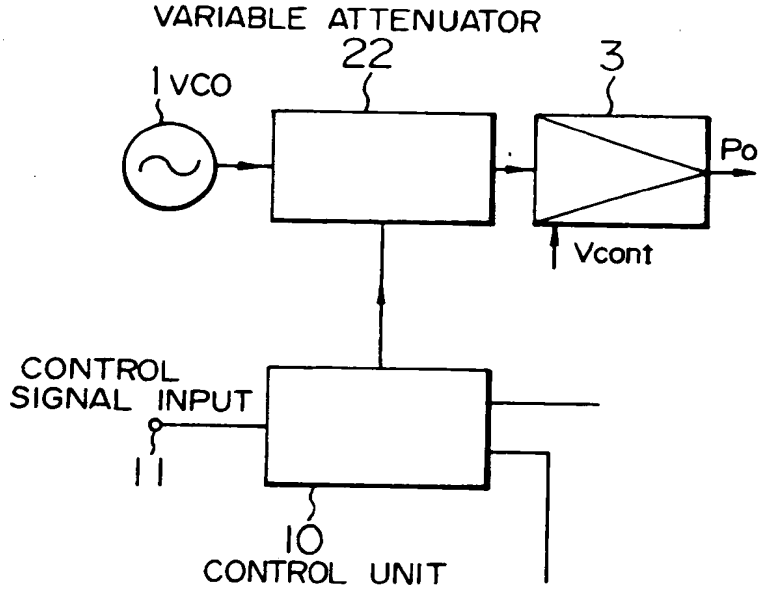

FIG. 11
PRIOR ART

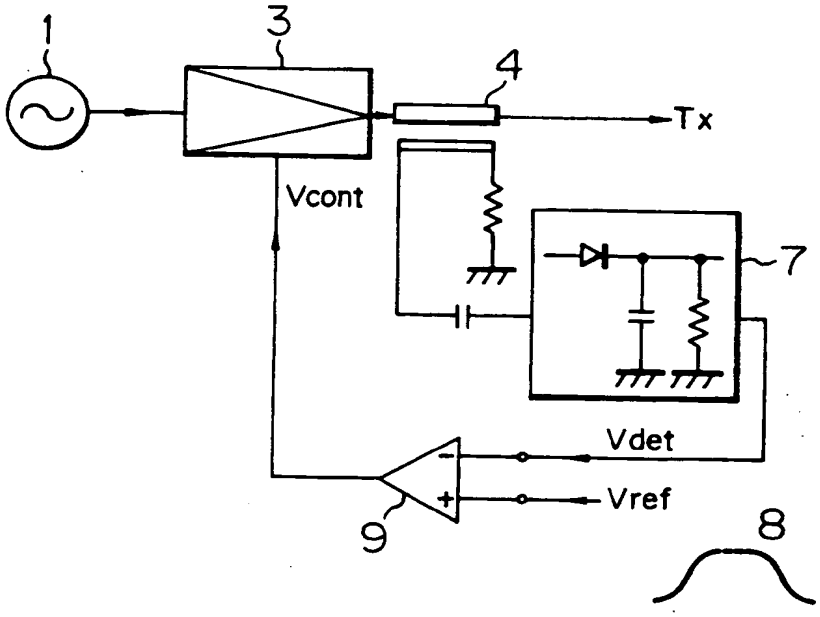

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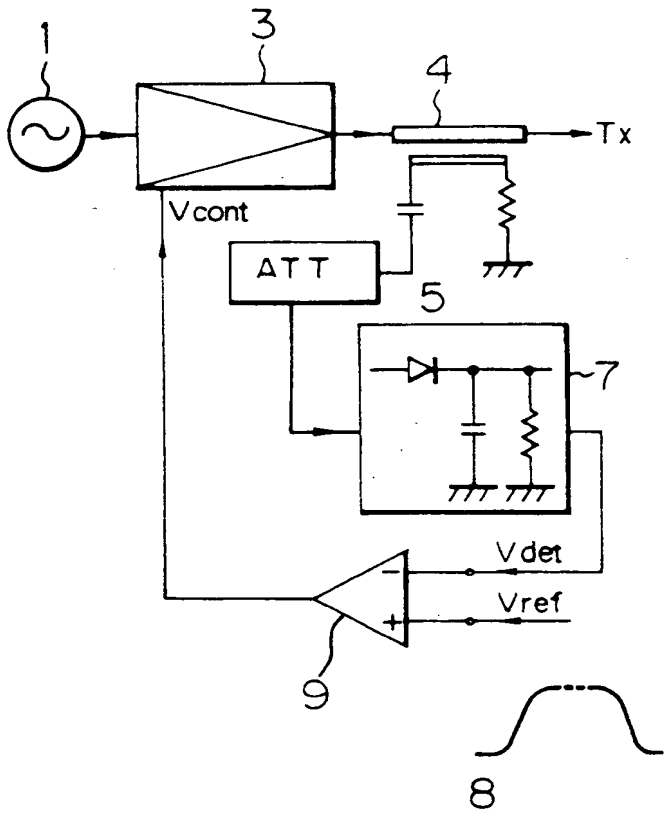
FIG. 12
PRIOR ART



BNSDOCID: <EP___0546693A1_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 31 0427

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 261 967 (NEC CORPORATION) * column 3, line 17 - line 25 * * column 3, line 49 - line 60 * * column 6, line 60 - column 8, line 62; figures 1-3 *	1,4-5,8, 11	H03G3/20
A	EP-A-0 369 135 (MOTOROLA INC.) * column 1, line 30 - column 3, line 11 * * column 3, line 28 - column 4, line 51; figure 1 *	1,4-5,8, 11	
P,A	EP-A-0 509 733 (MITSUBISHI DENKI KABUSHIKI KAISHA) * column 3, line 11 - column 4, line 43; figures 1-3 *	1,4-5,11	
P,A	EP-A-0 472 330 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD) 26 February 1992 * column 4, line 4 - column 5, line 49; figure 2 * D & JP-A-4 100 426 (...)	1,4-5,11	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5) H03G H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 MARCH 1993	DECONINCK E.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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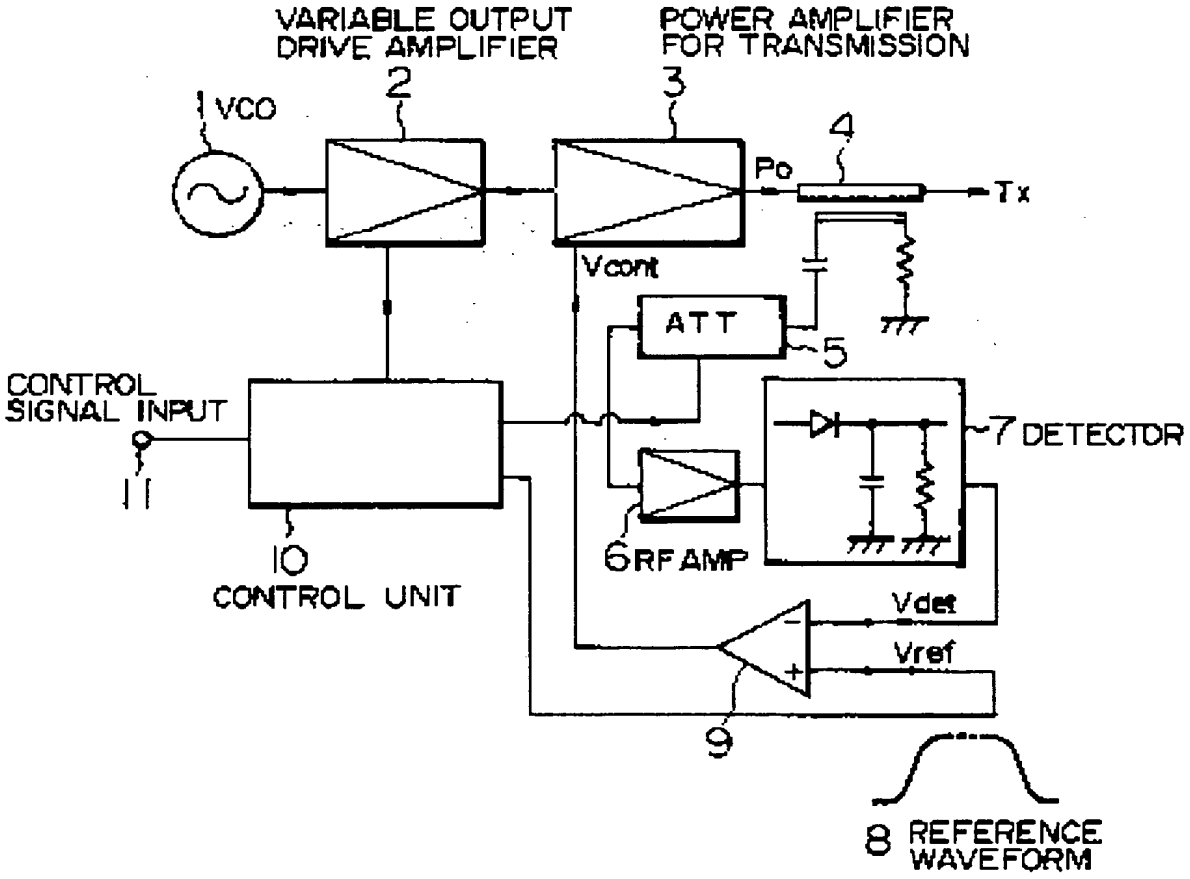
FIG. 1



BNSDOCID: <EP___0546693A1TI_>

FIG. 2

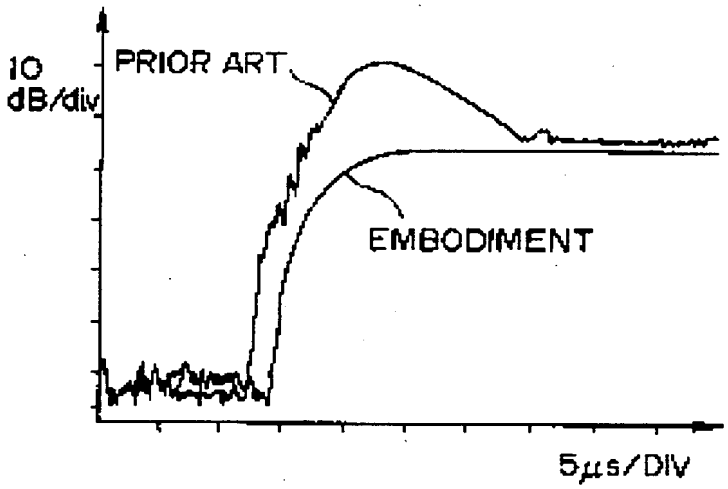


FIG. 3

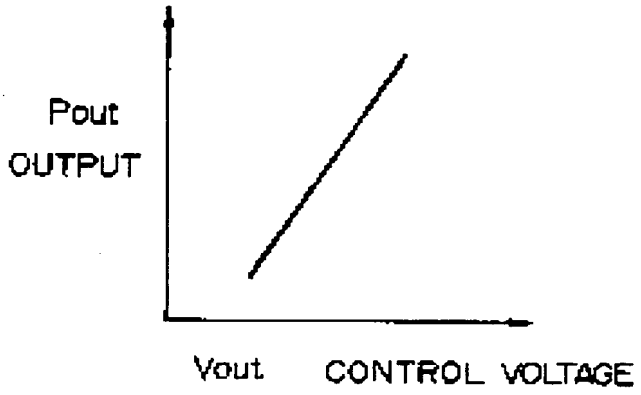


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FIG. 8

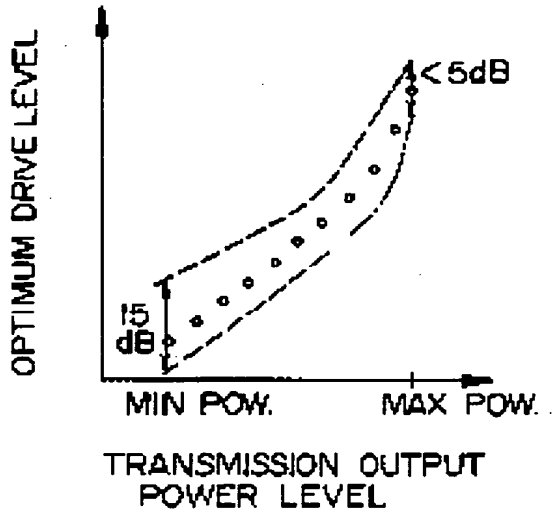
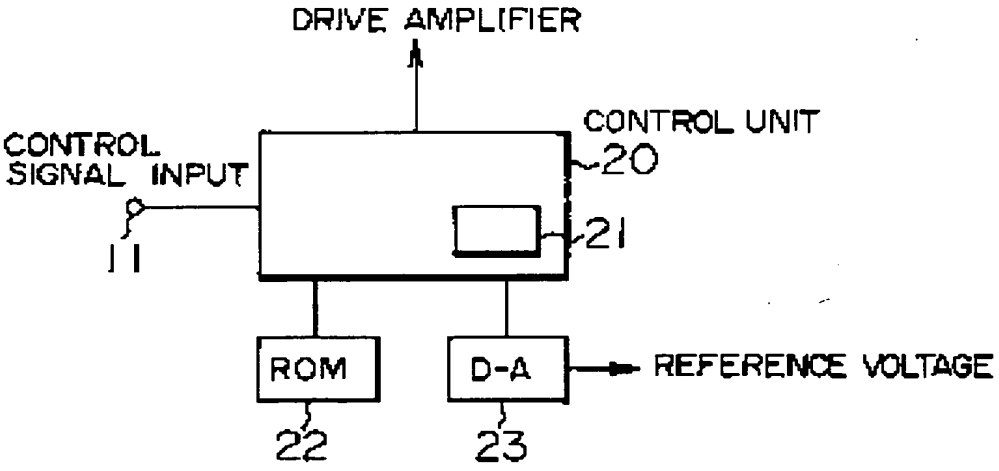


FIG. 9



BNSDOCID: <EP___0546693A1TI_>

FIG. 10

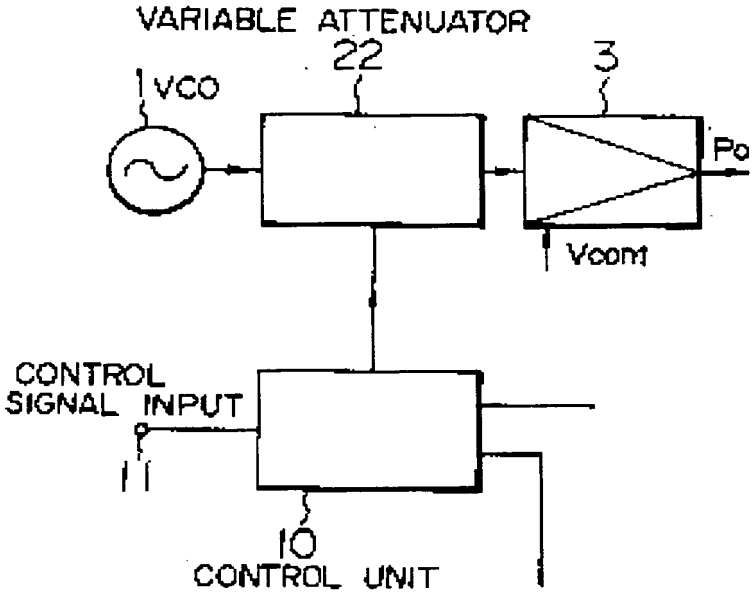
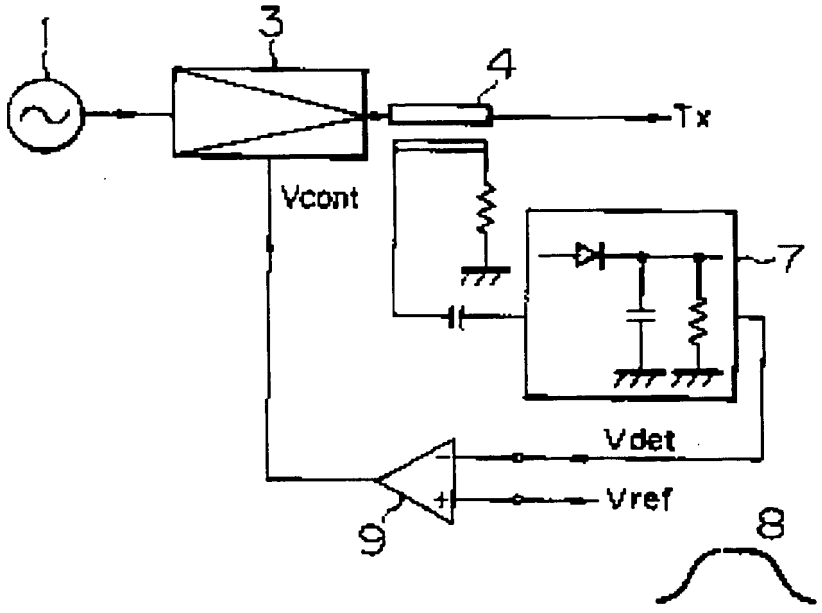


FIG. 11

PRIOR ART



BNSDOCID: <EP___0546693A1TI_>

FIG. 4

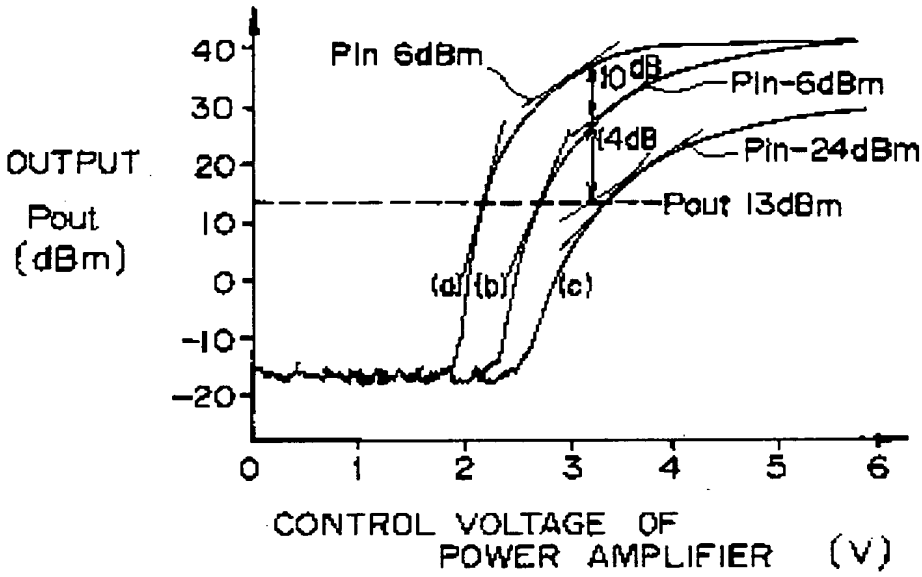
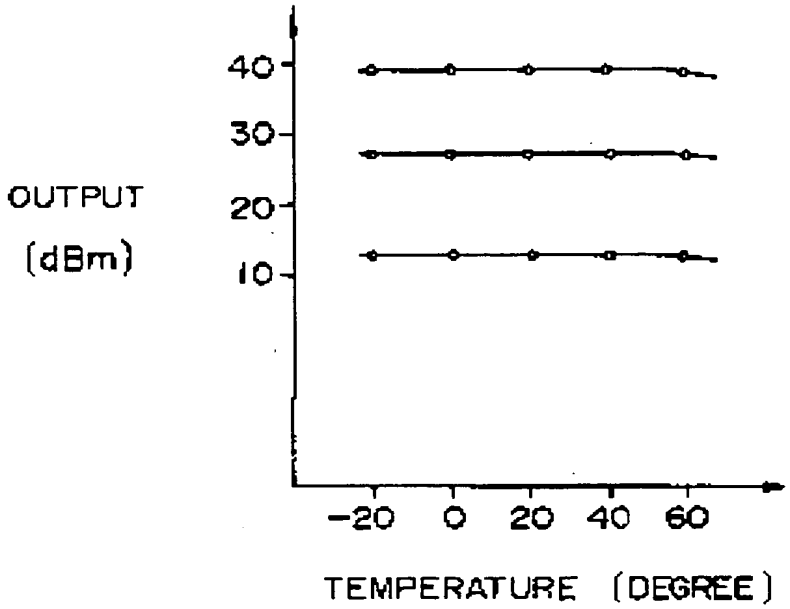


FIG. 5



BNSDOCID: <EP___0546693A1TI_>

FIG. 6

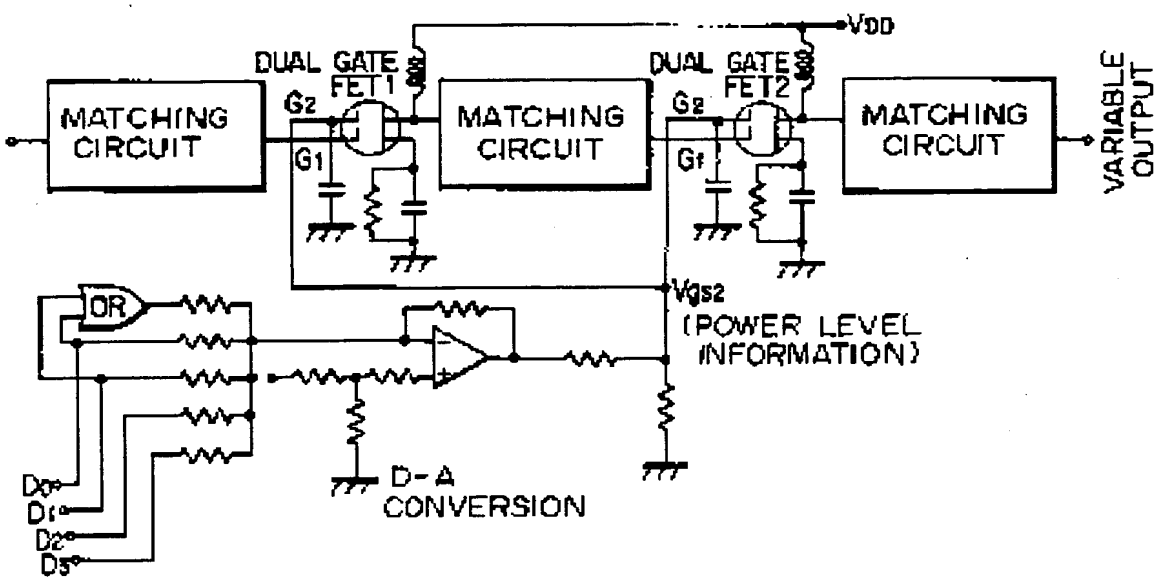
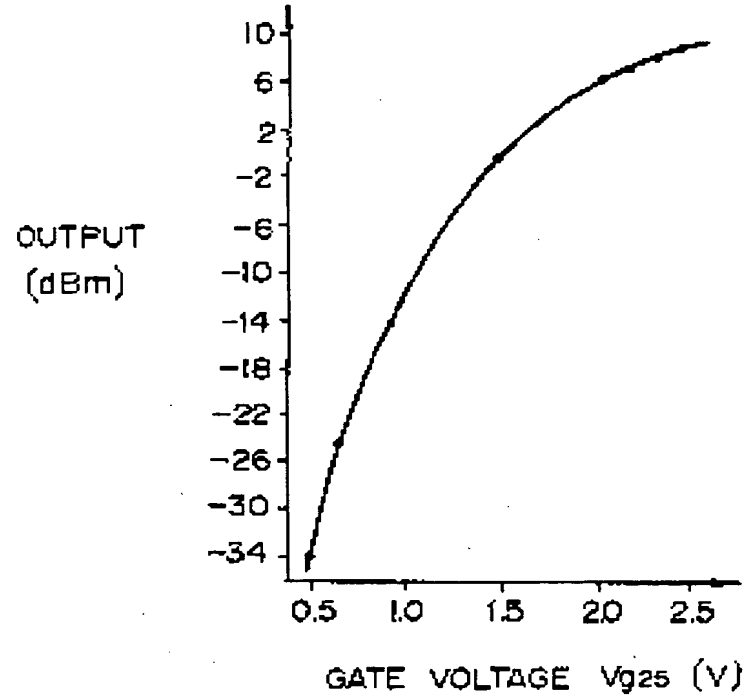
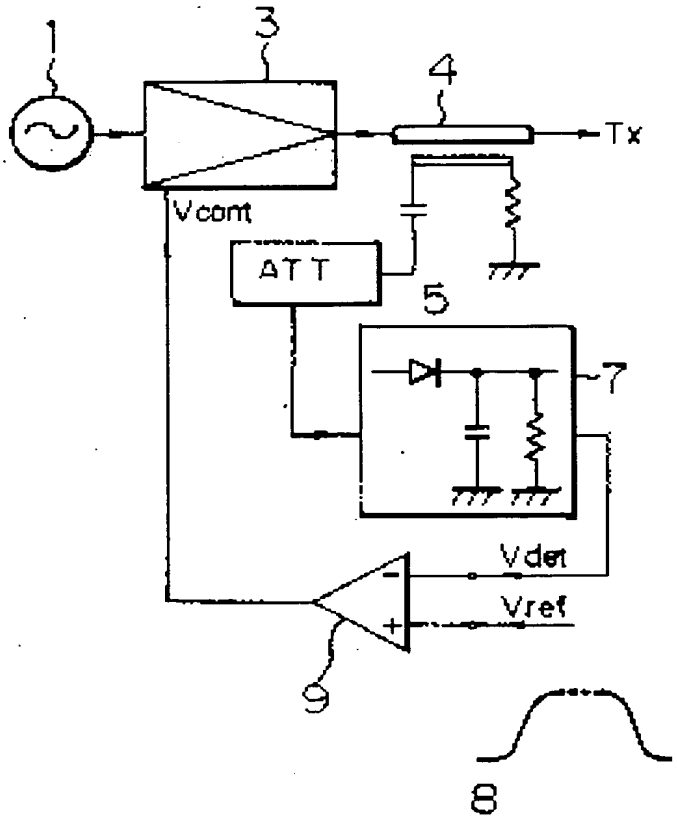


FIG. 7



BNSDOCID: <EP___0546693A1TI_>

FIG. 12
PRIOR ART



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